AMENDMENTS TO THE CLAIMS

This listing of claims replaces all previous versions and listings of claims in this application.

Claim Listing:

Claims 1-11: (Canceled).

12. (Previously presented) An apparatus for reducing the latency between stages of a pipelined processor, the apparatus comprising:

an instruction cache producing a plurality of instructions for execution by said pipelined processor;

a plurality of decode stages connected to receive the plurality of instructions from said cache;

an instruction queue having a plurality of locations, wherein one of the plurality of locations is configured to receive an associated instruction and a valid bit; and

a multiplexer associated with said one of the plurality of locations,

wherein, depending on a value of the valid bit, said multiplexer supplies said one of the plurality of locations in the instruction queue with either an output of one of the decode stages or an output of the instruction cache,

wherein, when the output of the instruction cache is supplied to said one of the plurality of locations in the instruction queue, the output of the instruction cache is simultaneously supplied to said one of the decode stages.

13. (Previously presented) The apparatus according to claim 12, wherein said multiplexer receives a shift signal for said instruction queue which shifts contents of said instruction queue towards an output port of said instruction queue, and which enables said instructions from said decoder to be transferred to said instruction queue.

14. (Previously presented) The apparatus according to claim 12, wherein said output port of said instruction queue is connected to a plurality of parallel processing stages.

15. (Canceled).